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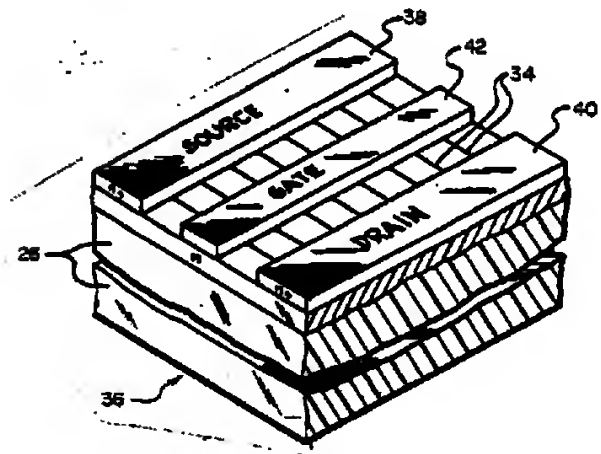
(54) Title: STRIPED-CHANNEL TRANSISTOR AND METHOD OF FORMING THE SAME

(57) Abstract

A striped-channel field effect transistor (FET) (36) in which a plurality of gate channels (34) extend through a semiconductor substrate (22) between a source (38) and drain (40). The channels (34) are laterally separated from each other by the substrate (22) material, and are doped to a substantially greater level than the intervening substrate (22) material. A gate (42) extends across the channels (34) and intervening substrate (22) material to control the effective channel cross-sectional areas as a function of the gate voltage. The channels are precisely formed by ion beam implantation (30). The channels (34) are surrounded by a depletion region as they approach pinchoff, thus giving the gate (42) greater control over the channel conductivity and a higher and more uniform device transconductance. The invention is applicable to both depletion and enhancement type FETs, and can be fabricated using a variety of processes.



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STRIPED-CHANNEL TRANSISTOR AND METHOD OF FORMING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to integrated circuit transistor structures, and more particularly to field effect transistors having a series of parallel channel stripes, and methods of forming the same.

Description of the Prior Art

An efficient form of field effective transistor (FET) has been developed in recent years which employs what is referred to as a castellated gate. In this type of device the channel is provided as a series of isolated channel stripes, each of which is subject to separate depletion or enhancement in accordance with the FET's operational mode. The aggregate surface area of the channels is collectively much greater than would be the case if a single channel covering an equivalent total area were used. This type of device is described in an article by R. C. Clarke, "A High-Efficiency Castellated Gate Power FET", Proceedings of the IEEE, IEEE/Cornell Conference on High-Speed Semiconductor Devices and Circuits, Cat. No. 83CH1959-6, August 1983, pages 93-111.

FIG. 1 illustrates the basic structure of a typical castellated gate FET. The device is formed using standard lithographic techniques and chemical etching. A series of parallel channels 2 formed from a relatively heavily doped

semiconductor material are provided on a substrate 4 of a much more lightly doped material. A metal gate 8 is flowed over each of the insulators 6 and down between adjacent insulators and channels 2, coming into contact with the channels along their lateral sides. The object is to progressively constrict the channels from both lateral sides as well as from above as the gate voltage approaches a pinchoff level.

A serious limitation of this prior art approach is that ideally the channel widths and depths should both be on the order of 100-200 nm and have a periodic spacing of 1 to 2 times this dimension for the channels to be fully constricted at the pinchoff voltage. With the lithographic and chemical etching techniques presently used to fabricate this type of device, channels this narrow are very difficult to attain on a reliable basis. Also, it is desirable that the FET's transconductance remain substantially uniform over the device's operating range, including operating near pinchoff as well as at high current levels (transconductance is defined as the change in drain current for a unit change in gate voltage at a given drain-source current). Unfortunately, the transconductance of the castellated gate device tends to vary as pinchoff is approached. Also, the surface is non-planar, which inhibits the use of short gate lengths.

SUMMARY OF THE INVENTION

In view of the above problems associated with the prior art, an object of the present invention is the provision of a novel and improved striped-channel transistor, and a method of forming the same, which has an improved construction over the prior art, can be readily fabricated to very small dimensions and exhibits a substantially uniform transconductance over its operating range, including the area near pinchoff.

Another object is the provision of such a transistor which is capable of operating with relatively small voltages as a consequence of its small dimensions.

These and other objects are accomplished in the present invention by means of an FET whose channel stripes are formed by focused ion beam implantation. A plurality of channels extend through a semiconductive substrate between a drain and source, with the channels laterally separated from each other by the substrate material. The channels are doped to a substantially greater level than the intervening substrate material. The effective channel cross-sectional areas are controlled as a function of a gate voltage signal by means of a gate which extends across the channels and the intervening substrate material.

The FET may be implanted as either a depletion or an enhancement device. In the depletion mode, the peak channel doping levels are in the approximate range of $1x10^{17}$ - $6x10^{18}cm^{-3}$; the corresponding doping levels are approximately $5x10^{16}$ - $5x10^{17}cm^{-3}$ for an enhancement device. In either case the substrate doping level is less than about $5x10^{15}cm^{-3}$.

The use of focused ion beam implantation enables the channels to be formed reliably and repeatedly to desired widths and depths, both within the range of about 100-200nm; the lateral spacing between adjacent channels can be accurately set within the desired range of 200-400 nm. When the substrate has a low doping level, the channels are formed by direct ion beam implantation into the desired channel tracks. The substrate may also have the desired channel doping level prior to formation of the channels, in which case the channels are formed by directing an ion beam onto the substrate areas lateral to the desired channel locations to reduce the doping of those areas to the desired substrate doping level.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of preferred embodiments, taken together with the accompanying drawings, in which:

DESCRIPTION OF THE DRAWINGS:

FIG. 1 is a fragmentary sectional view of the gate area in a prior art channel-striped transistor;

FIG. 2 is a simplified sectional view showing the direct formation of channels by a focused ion beam in accordance with the present invention;

FIG. 3 is a perspective view of an FET resulting from the channel formation illustrated in FIG. 2;

FIG. 4 is a sectional view of a single channel mapping the progressive constriction or expansion of the effective channel area in response to changes in the gate voltage;

FIG. 5 is a sectional view of a substrate with a doped layer which may serve as a base for the present invention;

FIG. 6 is a sectional view illustrating the formation of striped channels in the substrate of FIG. 5;

FIG. 7 is a perspective view of an FET resulting from the channel formation shown in FIG. 6; and

FIG. 8 is a graph of a set of drain I-V curves for incremental values of gate voltage, illustrating the substantially constant transconductance achieved by the present invention even in the pinchoff region.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring first to FIG. 2, a substrate wafer of semiconductive material such as gallium arsenide (GaAs) 10 is shown as a base for the FET of the present invention. GaAs is preferred because of its high speed capabilities,

and makes the present FET suitable for use in satellite microwave receivers in which low noise and large gain-bandwidths are required, and in digital signal processing for radar and communication systems where high speed is necessary. However, other semiconductive materials such as silicon or indium phosphide could also be used.

A focused ion beam 12 is illustrated as being applied to a channel area 14 formed into the upper surface of the substrate. Focused ion beam accelerators are well known, and are capable of focusing an ion beam to the small dimensions required by the present device. Silicon or other suitable materials can be used to provide the dopant. Although the device is illustrated as having n-type dopant, it should be understood that p-type dopant would also be suitable if accompanied by a reversal of the applied gate voltage polarity.

The ion beam is scanned over the substrate to form a series of straight, parallel channels 14. The individual channel widths are preferably about 100-200 nm, with a periodic spacing of about 200-400 nm between successive channels. The implant energy is set so that the channels are formed to a depth of about 100-200 nm. The peak channel doping level is normally $2x10^{17}cm^{-3}$, and preferably within the approximate range of $1x10^{17}$ - $6x10^{18}cm^{-3}$.

The substrate is nominally undoped, but in practice the substrate material will generally come with some amount of doping or will acquire a doping during processing. Although the present invention relies upon a substantial differential between the doping levels of the channels and the adjacent substrate, it will tolerate a substrate doping level up to about $5x10^{18}cm^{-3}$.

A perspective view of the completed device is provided in FIG. 3. A source 16 and drain 18 are formed at opposite ends of the channel stripes 14 with a doping

level substantially greater than that of the channels. A FET with a length of 50 microns in a direction transverse to the channels will accommodate approximately 80-160 channels. The channel lengths only need to be equal to the gate length for self-aligned gate devices. Channel lengths can be longer for more self-aligned gate devices. Suitable source and drain contacts, such as Au/Ge, are also provided but are not shown in FIG. 3.

A gate 20 is formed over the channel area between the source and drain, straddling both the channels and the intervening portions of the substrate. Various materials may be used for the gate. a metal such as Ti/Pt/Au may be employed, in which case a Schottky junction is formed between the gate and the underlying semiconductive material. Alternately, a semiconductive material such as GaAs, silicon or indium phosphide could be employed for the gate, thus forming a p-n junction at the gate-channel interface. With indium phosphide, but not with GaAs, an oxide layer could be inserted between the gate and the underlying channels. A silicon MOS structure could be implanted as either a depletion, enhancement or inversion device. A p-n junction will generally work as well as a Schottky junction, but is more difficult to fabricate.

Referring now to FIG. 4, a cross-section of an individual channel stripe is shown to illustrate the effect of a varying gate voltage upon the effective channel area. In the example shown the channel doping level is $2x10^{17}cm^{-3}$ for a depletion device and $1x10^{17}cm^{-3}$ for an enhancement device, while the doping level of substrate 10 is $1x10^{14}cm^{-3}$ for both cases. The channel width and depth are each about 120 nm.

For a depletion-type device, the application of an increasing negative gate voltage will produce a depletion layer in the substrate and channel that progressively constricts the effective channel area. The depletion

regions for various gate voltages are indicated in FIG. 4 by the topographical-type lines. With zero gate voltage the depletion region extends only slightly down into the channel, but much more deeply into the surrounding substrate; this is a direct result of the much heavier channel doping relative to the substrate. A depletion region is formed with a zero gate voltage because the Schottky junction formed between the metallic gate and semiconductive substrate produces an inherent voltage differential across the junction of about -.75 volts. A p-n junction would also produce an inherent voltage differential, the magnitude of which would depend upon the bandgap of the semiconductive material employed; the voltage for GaAs is about -.75 volts. If an oxide layer is disposed over the substrate with a metallic gate contact, the metal-oxide interface will also produce an inherent voltage differential. Gate junctions could also be devised that do not have inherent voltage differentials. In any case, the applied gate signal can simply be adjusted to compensate for any voltage differential associated with the gate junction to yield the same FET depletion action.

As the gate voltage is made more negative for the depletion device, the depletion region in both the channel and in the substrate adjacent the channel also increase. At the higher gate voltage levels the substrate depletion region extends into the sides and bottom of the channel, such that the channel is effectively surrounded by a depletion region. This gives the gate a much greater control over the charge in the channel than is available in prior devices, and produces a higher and more uniform device transconductance. As the gate voltage continues to increase, the channel is eventually constricted to pinch-off.

The response of an enhancement type device to gate voltage is similar to that of a depletion type device.

The channel ion implant dose and the depth of implant are controlled so that the channel of an enhancement device is preferably pinched off, due to the inherent Schottky junction voltage differential, with a zero gate voltage. The effective channel area then expands as the gate voltage is increased and made more positive; the rate of expansion per unit change in gate voltage is greater than for a depletion type device because of the lower channel doping level in the enhancement device.

Several processes are available to fabricate this novel type of FET. With a conventional, non-self-aligned gate, planar process, alignment marks are first etched or metallized onto a wafer to delineate the FET area. The source and drain are then formed with a heavy implant from the focused ion beam (or conventioned implanter), followed by the formation of channel stripes between the source and drain with a lighter doping from the focused ion beam. The wafer is then capped with silicon oxide, silicon nitride or other suitable material, and annealed. Resist is opened over the source and drain by ultraviolet exposure and developer, and ohmic contacts are formed on the source and drain by optical lithography methods. the resist and overriding metal are then lifted off. As an optional step, a resist can be laid down over the device and then removed from the channel area to enable etching of the channels to adjust the channel resistance and pinchoff voltage. Finally, a gate contact is deposited using optical or other appropriate lithography techniques, followed by lifting off the resist or by metal etching methods.

In an alternate method of forming the channels, the wafer is coated with a resist and channel stripes exposed in the resist with an ion beam, electron beam or possibly optical lithography techniques. The resist is then developed, opening the stripe regions. The wafer is next

flooded with ions to implant the channels in the areas where the resist has been removed, followed by stripping the remaining resist from the wafer. Several self-aligning processes are also available to form the FEt. Typically, after alignment marks are placed on the wafer the focused ion beam is used to implant the channel atripes (but not the source and drain at this time). The gate metal is then deposited over the device, and a gate pattern defined using either optical or other lithography methods (e.g., electron beam). The gates are defined in the metal using appropriate pattern transfer methods. Next, the source and drain are implanted with the focused ion beam or with a conventional implanter to much heavier doping levels than the channels; the shadow of the gate mask defined the ends of the channels and their interface with the source and drain. The device is then capped (if GaAs is used) and annealed, followed by the deposit of source and drain ohmic contacts.

The invention is also adaptable to molecular beam epitaxy or vapor phase epitaxy substrates, such as the substrate 22 illustrated in FIG. 5. These structures have a nominally undoped or lightly doped base layer 24, with a much narrower medium doped layer 26 on top of the base layer and a heavily doped layer 28 on top of the medium doped layer. They can be formed with the doping level of the medium doped layer corresponding to the desired channel doping level, and the doping level of the heavily doped layer 28 corresponding to the desired source and drain doping levels.

To form the present channel-striped FET from this type of substrate, the heavily doped layer 28 is first removed from over the channel region. A focused ion beam 30 is then used to implant ions of opposite polarity to the substrate doping in the intervening portions 32 of the substrate lateral to the intended channel locations 34.

The ion implantation thus reduces the doping level of the substrate between the channels, and is controlled so that the intervening substrate doping level is reduced to below about $5x10^{15}cm^{-3}$. For n-doped substrates, B^+ ions can be implanted, for example, to reduce the intervening substrate doping level. Alternately, the channels can be formed by coating the substrate with a resist, opening the resist between the channels, and ion flooding the partially coated substrate to the desired doping level between the channels.

A complete device 36 formed in this fashion is shown in FIG. 7. The heavily doped layer on either side of the channels 34 forms the source 38 and drain 40. A gate 42 extends laterally over the channels between the source and drain.

The drain I/V curves for various values of gate voltage are present in FIG. 8 for a depletion device formed in accordance with the invention. The regular vertical spacing between the curves for equal increments of gate voltage, down to the pinchoff region, demonstrates the very high degree of transconductance uniformity achieved.

Experimental results have been obtained with a device having a 4 micron channel length and a 1.5 micron gate length. The channel conductance stripes were written with a 100 keV focused ion beam of Si^{++} with a stripe width of one beam width (less than 0.2 micron) and a stripe spacing of 0.2 to 0.5 micron. Best results were obtained for a stripe spacing of 0.4 micron where the average g_m for the whole FET was 108 mS/mm and the effective g_m in the stripes was 300 mS/mm. The value of f_T was estimated by measuring the capacitance at 1MHz; the value for the 0.4 micron stripe spacing was 11.5 GHz, about 40% more than that with uniformly doped channels of the same dimensions. the results also show that the value of g_m is relatively

constant with decreasing drain current down to currents near pinchoff. This means that at the lower drain currents the device has a transconductance that is about 70% more than that obtained with a uniformly doped channel.

Results were also obtained for devices using the same mask set and similar starting material, but for which the gate and channel lengths were optical Self Aligned Gates (SAG). In these devices the SAG gates were about 1 micron in length with about 0.1 micron undercut. The current-voltage characteristic for these devices indicate higher output conductance, by a factor of two or more, compared with conventionally made MESFETs (on the same wafer), and a transconductance of 240 mS/mm. This is the total for the device; the transconductance in the stripes would be about 2 to 5 times this amount. Measurements of the gate-source capacitance indicate a gain bandwidth product, f_T, in the range of 12 to 15 GHz, or 15 - 20% higher than conventional MESFETs of the same dimensions.

While particular embodiments of the invention have been shown and described, it should be understood that numerous modifications and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

WE CLAIM:

1. A field effect transistor (FET), comprising:
a semiconductive substrate,
a source and drain on the substrate,
a plurality of channels extending through the substrate between the source and drain and laterally separated from each other by substrate material, the channels being doped to a substantially greater level than the intervening substrate material, and
a gate extending across the channels and the intervening substrate material, the gate controlling the effective channel cross-sectional areas as a function of the gate voltage.

2. The FET of claim 1, the channel doping levels being selected so that the effective channel cross-sectional dimensions in all directions vary as a function of the gate voltage.

3. The FET of claim 1, implemented as a depletion mode device in which the channel and substrate doping levels are selected so that a depletion layer is formed in the substrate around each channel and expands at a significantly greater rate than does a depletion layer in the channels as the gate voltage is increased in the doping polarity.

4. The FET of claim 3, wherein the peak channel doping levels are in the approximate range of $1x10^{17}$-$6x10^{18}cm^{-3}$.

5. The FET of claim 4, wherein the substrate doping level is less than about $5x10^{15}cm^{-3}$.

6. The FET of claim 1, implemented as an enhancement mode device in which the channel and substrate doping levels are selected so that the effective channel area increases as the gate voltage increases opposite to the doping polarity.

7. The FET of claim 6, wherein the peak channel doping levels are in the approximate range of $5x10^{16}$-$5x10^{17}cm^{-3}$.

8. The FET of claim 7, wherein the substrate doping level is less than about $5x10^{15}cm^{-3}$.

9. The FET of claim 1, wherein the channels are formed in the substrate by focused ion beam implantation.

10. The FET of claim 9, wherein the substrate prior to formation of the channels has the desired channel doping level, and the channels are formed by focused ion beam implantation to the desired substrate doping level in the substrate lateral to the channel areas.

11. The FET of claim 1, wherein the channels are formed in the substrate by coating the substrate with a resist, opening channel stripes in the resist, and ion flooding the partially coated stripes.

12. The FET of claim 1, wherein the substrate prior to formation of the channels has the desired channel doping level, and the channels are formed by coating the substrate with a resist, opening the resist between the channels, and ion flooding the partially coated substrate to the desired substrate doping level in the substrate between the channels.

13. The FET of claim 1, wherein the individual channel widths are approximately 100-200 nm.

14. The FET of claim 13, wherein the lateral spacing between adjacent channels is approximately 200-400 nm.

15. The FET of claim 13, wherein the channel depths are approximately 100-200 nm.

16. The FET of claim 1, said gate forming a Schottky contact with the channels and intervening substrate material.

17. A method of forming a field effect transistor (FET) on a semiconductive substrate, comprising:

forming a plurality of spaced, generally parallel channels in the substrate that connect the source and drain areas, the channels being provided with substantially greater doping levels than the intervening substrate material,

forming a source and drain in the source and drain areas, respectively, and

forming a gate over the channels and the intervening substrate material.

18. The method of claim 17, the substrate having a doping level substantially less than the desired channel doping levels, wherein the channels are formed by direct focused ion beam implantation along the channels to the desired doping levels.

19. The method of claim 17, the substrate having the desired channel doping level prior to formation of the channels, wherein the channels are formed by directing a focused ion beam onto the substrate areas lateral to the

desired channel locations to reduce the doping of those areas to the desired substrate doping level.

20. The method of claim 17, the substrate having a doping level substantially less than the desired channel doping level, wherein the channels are formed by coating the substrate with a resist, opening channel stripes in the resist, and ion flooding the partially coated substrate.

21. The method of claim 17, the substrate having the desired channel doping level prior to formation of the channels, wherein the channels are formed by coating the substrate with a resist, opening the resist between the channels, and ion flooding the partially coated substrate to the desired substrate doping level in the substrate between the channels.

22. The method of claim 17, wherein the channels are formed approximately 100-200 nm wide.

23. The method of claim 22, wherein the channels are formed approximately 100-200 nm deep.

24. The method of claim 22, wherein the channels are formed with lateral spacings between adjacent channels of approximately 200-400 nm.

25. The method of claim 17 for a depletion mode device, wherein the channels are formed with peak doping levels in the approximate range of $1x10^{17}$ - $6x10^{18}cm^{-3}$.

26. The method of claim 17 for an enhancement mode device, wherein the channels are formed with peak doping levels in the approximate range of $5x10^{16}$ - $5x10^{17}cm^{-3}$.

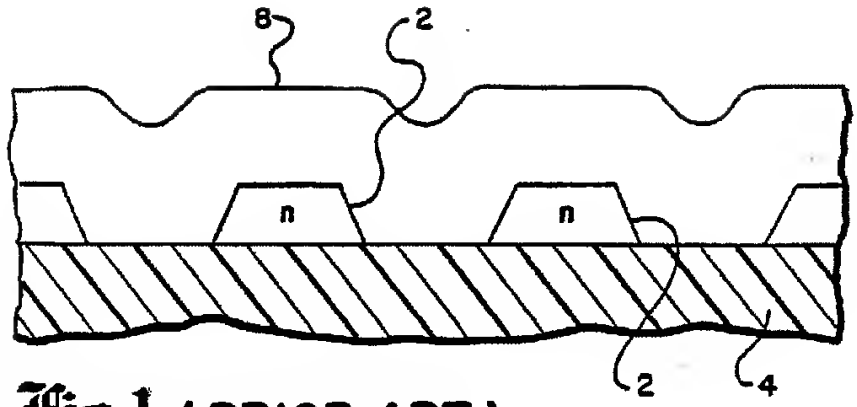


Fig.1. (PRIOR ART)

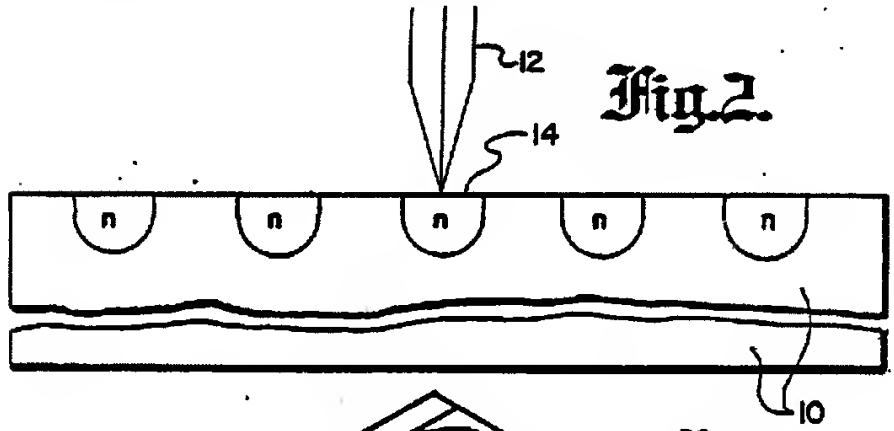


Fig.2.

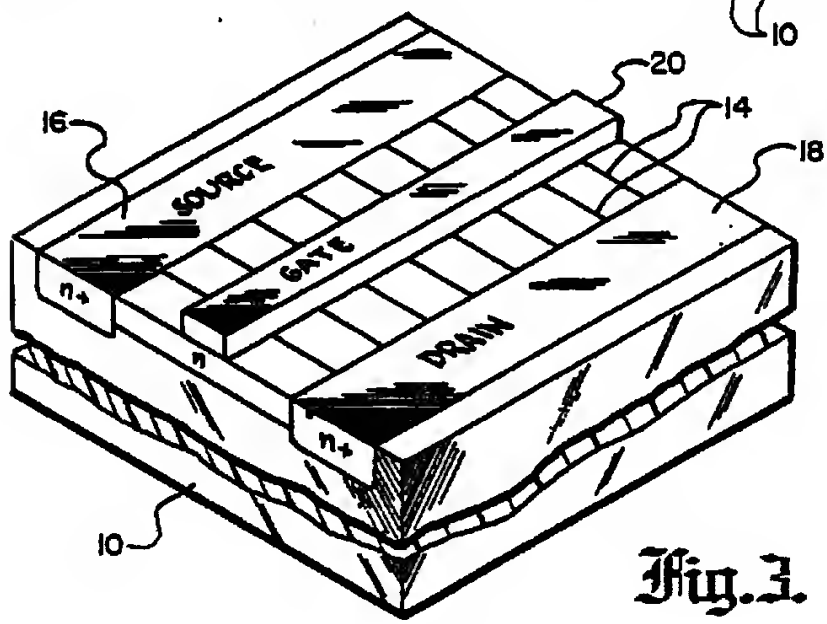
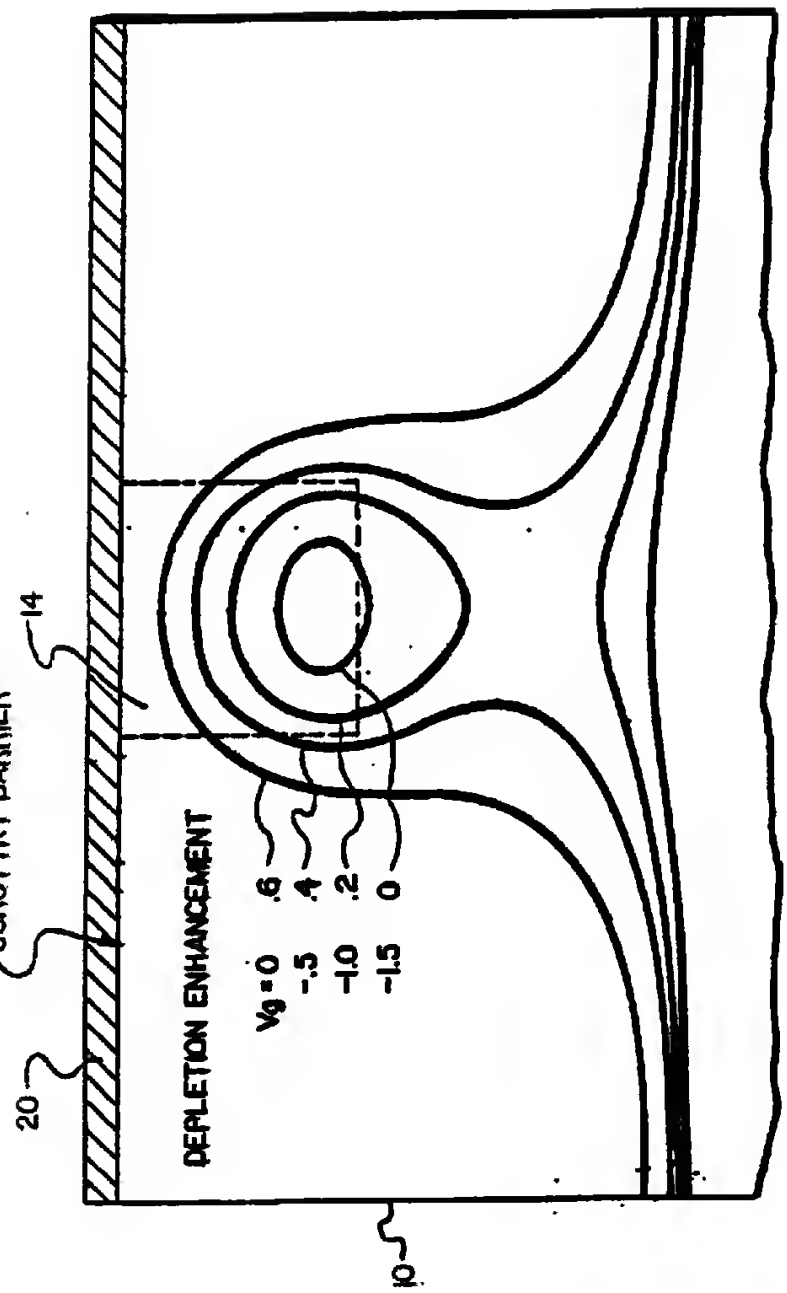


Fig.3.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DEPLETION ENHANCEMENT
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Fig. 4.

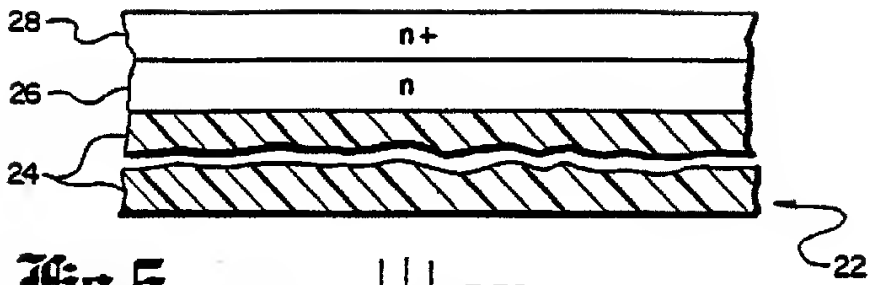

Fig.5.

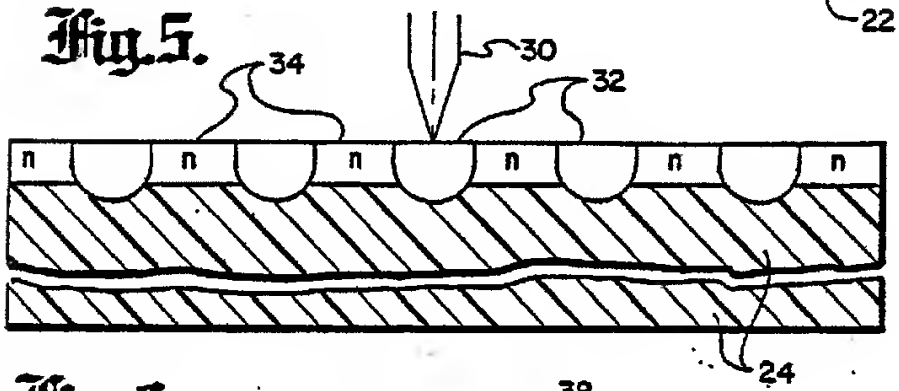

Fig.6.

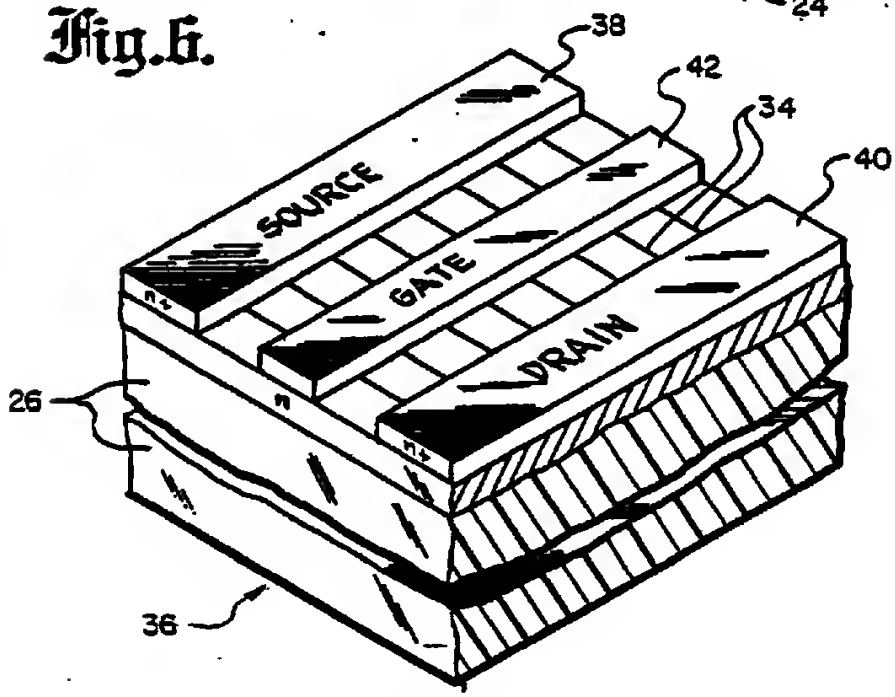

Fig.7.

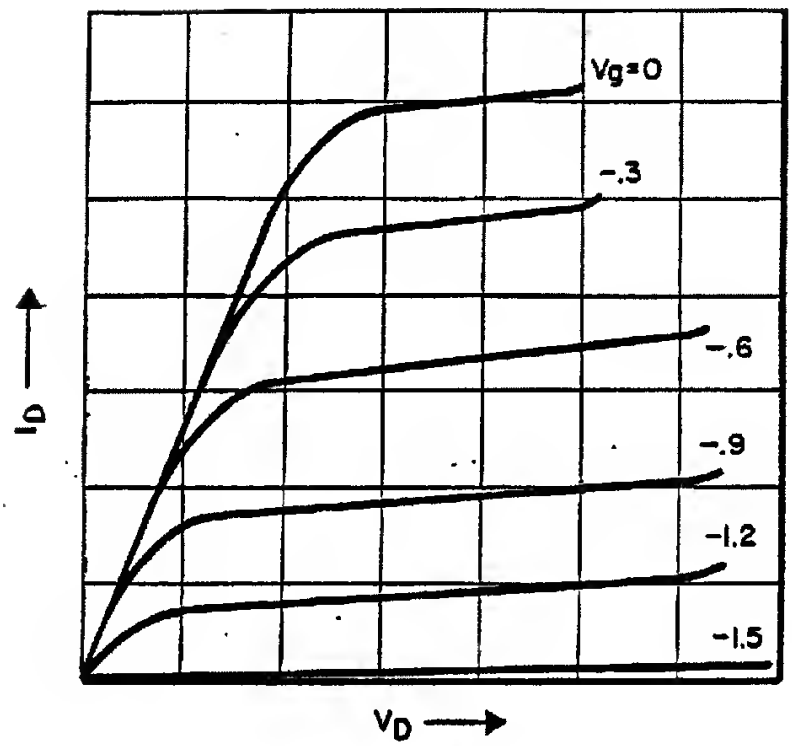

Fig.8.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/02379

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 29/10

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	Patent Abstracts of Japan, vol. 9, no. 295 (E-360)(2018), 21 November 1985 & JP, A, 60134468 (HITACHI SEISAKUSHO K.K.) 17 July 1985 see abstract; figures --	1,3,9,17,18
A	EP, A, 0167810 (EATON CORP.) 15 January 1986 see page 2, line 9 - page 3, line 4; page 5, line 13 - page 6, line 17; figure 1 --	1-3,5
A	FR, A, 1306187 (WESTINGHOUSE ELECTRIC CORP) 3 September 1962 see page 2, left-hand column, last line - page 3, left-hand column, line 20; figure 3 --	1
A	EP, A, 0011879 (SIEMENS AG) 11 June 1980 see page 7, lines 15-31; figure 6 --	1,2
A	International Electron Device Meeting Technical Digest, 5-7 December 1983,	./.

* Special categories of cited documents: [14]

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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
14th March 1988	14 APR 1988
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category*	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8702379 SA 19908

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 30/03/88
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